A PAM-4 Adaptive Analog Equalizer with Decoupling Control Loops for 25-Gb/s CMOS Serial-Link Receiver

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Abstract—PAM-4 signaling is an effective solution for high-speed CMOS serial-link transceivers, but it suffers from the difficulty of signal regeneration in analog front-end owing to its multi-level characteristics. An adaptive analog equalizer with decoupling control loops is proposed to address the nonlinearity of amplifiers. A low-frequency gain invariant equalizer and a golden signal generator are designed to serve boost and swing control loops, respectively. An integrating charge pump is employed to improve the convergence performance of receiver. Transistor-level simulation results show that the proposed adaptive analog equalizer in 40-nm CMOS technology can recover 25 Gb/s random data transmitted over a 29.8 inches Megtron6 printed circuit board (PCB) copper channel.

I. INTRODUCTION

The operating frequency of modern high-capacity storage, networking, and data processing systems increases rapidly. Due to frequency-dependent impairments such as skin effect and dielectric loss, high-speed data transmission suffer from severe inter-symbol interference (ISI) [1]. To eliminate the ISI and improve the bit error rate (BER), analog equalizers [2]–[5] have been employed in the front-end equalization due to its low cost and high boost in Nyquist frequency. Nowadays, multi-level signaling technique, such as four-level pulse amplitude modulation (PAM-4), has been widely adopted in high-speed transceivers [6]. Because PAM-4 signaling technique can achieve double data rates theoretically [7], [8] under a given band-limited channel. A combination of analog equalization and PAM-4 signaling is supposed to be an effective solution for high-speed transceivers.

Despite the efficiency of PAM-4 signaling is at the expense of more circuit design difficulties. Traditionally, amplifiers regenerate signals from small swing, but non-ideal amplifiers will not keep a constant gain as the input signal increasing, because the working point of the amplifier no longer satisfy the small-signal model, as shown in Fig. 1. In other words, the gain of the outer level will less than the inner level when the inputting PAM-4 signal is too large, which will distort the PAM-4 eye diagrams and have serious implication on the average signal-to-noise ratio (SNR). We call this phenomenon the linear gain demand in PAM-4 signaling. The nonlinearity of amplifiers (or any differential pair based circuits) should be taken into consideration and careful swing control is needed during the design of analog front-end, especially the one with adaptive loops.

An adaptive equalizer architecture for Non-Return-to-Zero (NRZ) signaling was designed in a 10 Gb/s serial-link receiver [3]. In this circuitry, a limiting amplifier [4] was used to sharpen the equalized signal and generate a reference signal for the adaptive loop. However, this solution could not be simply applied to PAM-4 signaling, because the PAM-4 signal will be distorted after going through the limiting amplifier. To remove the impact produced by limiting amplifiers when adopting PAM-4 signaling, a 14 Gb/s PAM-4 adaptive analog equalizer was presented in [5]. This solution replaced the limiting amplifier with a two-bit slicer and a two-bit digital-to-analog converter (DAC). But its equalizer lacks a swing control loop, which may make the adaptive loop converge to non-ideal points.

To address the linear gain demand in PAM-4 signaling, this paper proposes an adaptive analog equalizer for PAM-4 signaling with decoupling control loops adjusting the boost and swing levels. To reduce the uncertainties in the boost...
control loop, the proposed analog equalizer is designed to be low-frequency gain invariant, while its high-frequency boost is controlled by the voltage, decoupling the swing control from the boost control loop, and ensuring that the swing of equalized signal falls in the linear region. Different from conventional adaptive loops, the proposed swing-control loop uses a golden signal generator other than amplifiers to adjust the swing, which alleviates the distortion of the reference signal produced by non-ideal amplifier and satisfies the linearity of PAM-4 signaling. To improve the convergence accuracy, an integrating charge pump circuit with high output resistance is also employed.

The rest of this paper is organized as follows. Section II describes the existing schemes of adaptive analog equalizers and our solution. Section III presents the circuit designs of adaptive equalizer in detail. Section IV gives the experimental results and finally Section V concludes.

II. ADAPTIVE ANALOG EQUALIZER

A. NRZ Adaptive Analog Equalizer

In the adaptive analog equalization circuits for NRZ signaling [3], a RC-degenerated differential pair is used to cope with channel attenuation while a limiting amplifier and a variable gain amplifier (VGA) are used as a slicer to sharpen the equalizer outputs. The adaptation loop adjusts the peaking according to the difference between high-frequency contents of the data before and after slicing, as shown in Fig. 2.

The amount of boost of RC-degenerated differential pair is proportional to distance between the zeros and the poles, while low-frequency gain is degenerated by the same factor [9]. When the high-frequency boost control voltage is varying to find an optimal operation point, both low-frequency gain and high-frequency boost are changing, which will add uncertainties to the control loop. Even if a complex design can be done to maintain the stability of the loop, considering the linear gain demand in PAM-4 signaling, the limiting amplifier and VGA will slice the PAM-4 signal into two levels and can no longer generate a perfect signal for comparison.

B. PAM-4 Adaptive Analog Equalizer

The receiver in [5] for PAM-4 signaling, generated the reference signal by replacing the limiting amplifier with a two-bit slicer and a two-bit DAC. But its equalization lacks a swing control loop, as shown in Fig. 3(a), which may make the loop converge to a non-ideal working point. With a certain control voltage, the equalized data shows no ISI but a swing larger than the reference, as illustrated in Fig. 3(b). The loop continues to decrease the boost since the power of equalized signal is still larger than that of reference. The output data will contain ISI in the steady state because further decreasing the boost of the equalizer attenuates the high-frequency content of data while amplifying the low-frequency content of data [9]. The problem in designing a swing-control loop is how to generate a PAM-4 reference signal with controllable swing and keep its linearity.

C. Proposed PAM-4 Adaptive Analog Equalizer

To attack the issues above, our proposed adaptive equalization receiver architecture with decoupled loops is shown in Fig. 4. The proposed analog equalizer is designed to be low-frequency gain invariant, while its high-frequency boost is controlled by a control voltage, coping with the channel loss. The pre-amplifiers slice the equalized signal into three logic levels, which are sampled and decoded by the following latches and a decoder, generating two-bit digital output. A golden signal generator with controllable swing is designed to generate suitable reference signal for comparison in the boost control loop. Power comparator with high-pass filters or low-pass filters is employed to compare the equalized signal with the golden signal, obtaining feedback signals for the control loops. An integrating charge pump is designed to accumulate the feedback signals and maintain the DC voltages for controlling. High-frequency contents of golden reference signal and signal after analog equalizer are compared in a boost control loop, while low-frequency contents are compared in a swing control loop. Decoupling the swing variation from...
III. ADAPTIVE ANALOG EQUALIZER CIRCUIT DESIGN

A. Low-frequency Gain Invariant Equalizer

To obtain enough gain bandwidth product, the proposed analog equalizer consists of three stages RC-degenerated differential pair, as shown in Fig. 5. The transfer function of the low-frequency gain invariant equalizer is given by

$$H(s) = \frac{(g_m R_L)^3}{(jw R_L C_p + 1)^3} \cdot \frac{j w R_1 C_{s1} + 1}{j w R_1 C_{s1} + 1 + g_m R_1} \cdot \frac{j w R_3 C_{s3} + 1}{j w R_3 C_{s3} + 1 + g_m R_3} \cdot \frac{1}{1 + g_m R_{s2}},$$ \hspace{0.5cm} (1)

where $R_L$ and $C_p$ represent the load resistances and parasitic capacitances of the differential pair in the next stage, respectively, and $g_m$ denotes the transconductance of the transistors in the present stage. All stages employ the same $R_L$, bias current, and length-width ratio of transistors to set an uniform $g_m$ and an identical far-end pole at $|w|_{p2} = 1/(R_L C_P)$. The control voltage $V_{ctrl}$ sets the capacitances of $C_{s1}$, $C_{s3}$, and the gate voltage of $N_1$ directly, and is converted into a reverse version by transistor $N_{bias}$ and bias resistors ($R_{bias1}$ and $R_{bias2}$) to set the gate voltage of $N_2$. According to the transfer function of low-frequency gain invariant equalizer, the low-frequency gain is given by

$$H(0) = \frac{(g_m R_L)^3}{(1 + g_m R_{s1})} \cdot \frac{1}{(1 + g_m R_{s2})} \cdot \frac{1}{(1 + g_m R_{s3})},$$ \hspace{0.5cm} (2)

where $R_{s1}$ consists of a transistor $N_1$ and a resistor $R_1$, and $R_{s2}$ consists of a transistor $N_2$ and a resistor $R_2$. The resistance of $R_{s1}$ is negatively associated with the control voltage, while the resistance of $R_{s2}$ is positively associated with it. Therefore low-frequency gain can keep constant under careful parameters setting when the control voltage is changing.

B. Pre-amplifiers and Decoder

PAM-4 signal after the analog equalizer should be sliced and decoded into two-bit data, as illustrated in Fig. 6. Three pre-amplifiers [5] compare signals with different reference signals ($V_{up}$, $V_{cm}$, and $V_{down}$), which are generated by a golden signal generator (discussed in subsection III-C), preparing for the sampling of latches. Signals digitized by pre-amplifiers and latches are decoded by decoder, obtaining the Most Significant Bit (MSB) and the Least Significant Bit (LSB).

C. Golden Signal Generator

The golden signal generator plays the role of generating a perfect PAM-4 signal with controllable amplitude for comparison in both high-frequency boost control loop and the swing-control loop. Using conventional amplifiers to control the swing of reference signal is too difficult to meet the linear gain demand, while using DAC will be limited by the operation rate and the footprint overhead. Another issue is how to provide reference levels automatically for pre-amplifier decision, as discussed in subsection III-B. For this reason, we design a current-steering based golden signal generator with controllable resistor loads as shown in Fig. 7.

The common mode voltage is maintained by two fixed resistors $R_L$ and a total bias current of $3I$, which can be expressed in

$$V_{cm} = V_{cc} - 1.5 \cdot R_L \cdot I.$$ \hspace{0.5cm} (3)
And the load resistance of the small-signal model can be expressed in

\[ R_{\text{load}} = R_L \|(R_d + R_{\text{on}}/2). \] (4)

Here \( R_{\text{on}} \) represents the resistance of PMOS transistor \( P_1 \), which is controlled by the swing-control voltage. The two-bit digital signals (MSB, LSB) control the flow directions of the current to produce four-level voltages \( (V_{\text{cm}} + 3 \cdot R_{\text{load}} \cdot I), (V_{\text{cm}} + R_{\text{load}} \cdot I), (V_{\text{cm}} - R_{\text{load}} \cdot I), \) and \( (V_{\text{cm}} - 3 \cdot R_{\text{load}} \cdot I). \) It is necessary to mention that the resistance of transistor is not only affected by the gate voltage, but also the source-drain voltage, which will make slight influence in PAM-4 signal linearity. After adding two resistors \( R_d \) to both sides of \( P_1 \), reducing the amount of source-drain voltage variation, this influence becomes negligible.

This generator circuit also has the advantage of producing reference levels adaptively. By adopting the same load resistance control voltage, fixing digital inputs, and changing the steering currents into \( 2.5I \) and \( 0.5I \), the reference level generation is done with same common mode voltage. Its appropriate reference levels are given by

\[ V_{\text{up}} = V_{\text{cm}} + 2 \cdot R_{\text{load}} \cdot I \]
\[ V_{\text{down}} = V_{\text{cm}} - 2 \cdot R_{\text{load}} \cdot I. \] (5)

D. Power Comparator

The power comparator compares the high or low frequency power of equalized signal and the golden signal in the boost-control loop or the swing-control loop, respectively. Two first-order high-pass RC filters distill the high-frequency contents from inputs in the boost-control loop, while two first-order low-pass RC filters distill the low-frequency contents in the swing-control loop. The high or low frequency components of equalized signal and golden signal convert themselves to power by steering the tail current \( I_{\text{SS}} \) through a four-transistor quad \( N_1 - N_4 \), and the output is smoothened by a capacitor \( C_2 \) [10], producing the feedback signal \( V_{fb} \), as shown in Fig. 8.

E. Integrating Charge Pump

The charge pump circuit pumps or drains current according to the output of power comparator, generating the corresponding DC voltage to determine the boost level of analog equalizer or to determine the swing level of golden signal generator. The system becomes stable when the power of equalized signal and golden signal is equal, reaching the optimal state. However, the operation point of charge pump [5] can be easily affected by the output voltage. In other words, the system will never reach an optimal state, because the power comparator must provide a small differential input for charge pump to maintain the output control voltages. The imperfection of the integrating charge bump is inevitable, but modification in circuit increasing the output resistor of the charge pump will be helpful. In our charge pump design, we adopt regulated cascode structure [11] to increase the output resistor of the charge pump, as the shadow region shown in Fig. 9. This kind of current mirror has the advantage of high output resistance and its small-signal model can be also found in Fig. 5. Small-signal analysis shows that it achieves an output resistance on the order of \( g_m^2 \cdot R_{ds}^3 \), where \( g_m \) and \( R_{ds} \) represent transconductance and small-signal output resistance of the transistors, respectively. To obtain a symmetric structure and improve the stability of the charge pump, further transistors are added to the circuit, constituting three operational amplifiers, as the dotted transistors shown in Fig. 9.
The proposed adaptive analog equalizer is designed in 40-nm low leakage CMOS technology under EDA platform of Cadence. The simulation is performed on the transistor-level implementation of these circuits.

A. Circuit Performance

The frequency response of the low-frequency gain invariant equalizer is illustrated in Fig. 10. When the control voltage varies from 0.9 V to 0.3 V, the equalizer exhibits a boost range from 0 to 16 dB at 6.25 GHz, while the low-frequency gain maintains 0 dB, which ensuring the equalized signal falls in the linear region.

The transient simulation result of the proposed integrating charge pump is shown in Fig. 11. Affected by differential input \( V_{fb+} \) and \( V_{fb-} \), the dotted line represents the accumulate result of a conventional charge pump [5], while the solid line represents the result of the proposed integrating charge pump. Obviously, the conventional charge pump cannot maintain the integrating voltage, when the differential input signal becoming zero, while our circuit performs perfectly. In this way, the difference between equalized signals and golden signals can be reduced.

B. System Performance

Fig. 12 shows the simulation result of the adaptive equalizer working at 25 Gb/s data rate across an 29.8 inches Megtron6 channel [12]. Without swing decoupling, the changing low-frequency gain of the analog equalizer might probably make the swing of equalized signal exceed its linear region. Fig. 12(a) shows the eye diagram of the distorted signal, which suffers from the nonlinearity of amplifiers. The amplification stage in our proposed analog equalizer, tracking the DC level of first stage and maintaining reasonable swings is a good choice to attack the nonlinearity in PAM-4 signaling. The eye diagram in Fig. 12(b) shows good linearity when adopting decoupling loops, achieving an average eye height of 100 mV and an average eye width of 40 ps. Fig. 12(c) shows the eye diagram of the adaptive golden signal and its optimal reference decision levels (\( V_{up} \) and \( V_{down} \)) for pre-amplifiers when adopting decoupling loops. The exactly same swing of equalized signal in Fig. 12(b) and golden signal in Fig. 12(c) shows well convergence of the swing-control loop.

C. Convergence Analysis

We have also compared the convergence performance between a conventional charge pump [5] and the proposed integrating charge pump in our adaptive system. For convenience, we replaced the charge pump with the conventional one in the boost loop, while the swing loop still adopted our proposed one. The swing control voltage will first converge to a certain amount, corresponding to the low-frequency content of the equalized signal, because the swing control loop has been decoupled from the boost control loop, and the variant boost control voltage will not influence the swing control loop any
more, as the control voltages shown in Fig. 13.

The eye diagram when adopting the conventional charge pump is obviously over equalized, as shown in Fig. 14, which can be explained by the adaptive mechanism. In the boost control loop, if the high-frequency content of the equalized signal $P_{eq}$ is larger than the golden signal $P_{ref}$, the power comparator will generate feedback signal $V_{fb+} > V_{fb-}$, and the capacitor will be charged by the charge pump, increasing the boost control voltage, decreasing the high frequency boost, and vice versa. The optimal state is $P_{eq} = P_{ref}$, and $V_{fb+} = V_{fb-}$.

However, the power comparator must provide a small differential input for charge pump to maintain the output voltage, which means $P_{eq} \neq P_{ref}$ in the steady state. As a result, the average value of $|V_{fb+} - V_{fb-}|$ represents the convergence accuracy of the adaptive loop. Fig. 15 shows the feedback signals in the boost loop, when adopting the conventional charge pump (the dot line) and the proposed integrating charge pump (the solid line), and their mean values are 7.31 mV and 0.27 mV, respectively. Therefore, the proposed integrating charge pump can achieve higher convergence accuracy.

VI. CONCLUSION

An adaptive analog equalizer architecture is proposed for PAM-4 signaling in high-speed serial-link receiver. With new designs in the low-frequency gain invariant equalizer and the golden signal generator, we decouple the swing-control from the boost-control loop to attack the nonlinearity of amplifiers and adaptively implement PAM-4 signal regeneration. New designs in integrating charge pump improve the accuracy of the loop convergence. Simulation results show that the proposed PAM-4 adaptive analog equalizer can compensate at least 16 dB loss at 6.25 GHz, reaching a data rate of 25 Gb/s.

VI. ACKNOWLEDGMENTS

The authors would like to thank the anonymous reviewers for their comments and valuable suggestions, which have helped us to improve the quality of the paper. This work has been supported by Open Project Program of the State Key Laboratory of Mathematical Engineering and Advanced Computing under grant 2013A04, and the State Key Laboratory of High-end Server & Storage Technology under grant 2014HSSA12.

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